WHAT IS CLAIMED IS:

1. A method of fabricating a field-effect device on an integrated circuit, comprising the steps of:

providing a single-crystal silicon substrate;

forming a metal silicate dielectric layer on the substrate; and

forming a conductive gate overlying the metal silicate dielectric layer.

2. The method of claim 1, wherein the forming a metal silicate dielectric layer step comprises:

exposing a clean Si surface on the substrate;

depositing a first metal on the Si surface;

annealing the substrate in an inert ambient, thereby forming a layer of a silicide of the first metal on the substrate;

oxidizing the layer of a silicide of the first metal, thereby forming the metal silicate dielectric layer.

3. The method of claim 2, further comprising oxidizing less than 1 nanometer of the clean Si surface prior to the depositing a first metal step.

4. The method of claim 2, wherein the oxidizing step comprises simultaneous exposure of the layer of a silicide of the first metal to both an oxidizing gas and a reducing gas.

5. The method of claim 4, wherein the oxidizing gas is selected from the group consisting of O_2, H_2O, N_2O, CO_2, and combinations thereof.

6. The method of claim 4, wherein the reducing gas is selected from the group consisting of CO, H_2, CH_3, and combinations thereof.

7. The method of claim 4, wherein the oxidizing gas is selected from the group consisting of O_2, H_2O, N_2O, CO_2, and combinations thereof , and wherein the reducing gas is selected from the group consisting of CO, H_2, CH_3, and combinations thereof.

8. The method of claim 2, wherein the oxidizing step comprises exposure of the layer of a silicide to an oxygen plasma.

9. The method of claim 8, wherein the oxygen plasma is exposed to ultraviolet radiation.

10. The method of claim 2, further comprising annealing the metal silicate layer in a non-oxidizing environment, thereby densifying the silicate layer.

11. The method of claim 10, wherein the annealing step is carried out at a temperature sufficient to crystallize the silicate layer.

12. The method of claim 1, wherein the forming a metal silicate dielectric layer step comprises:

depositing a first metal on the substrate in an oxidizing ambient, thereby forming an at least partially oxidized layer on the substrate; and

annealing the substrate in an oxidizing ambient.

13. The method of claim 12, wherein the substrate comprises an oxidized silicon surface layer immediately prior to the depositing step.

14. The method of claim 12, wherein the substrate comprises a clean Si surface immediately prior to the depositing step.

15. The method of claim 12, wherein the depositing a first metal step comprises sputtering material from a target of the first metal onto the substrate.

16. The method of claim 1, wherein the forming a metal silicate dielectric layer step comprises:

depositing a first metal and silicon on the substrate in an oxidizing ambient, thereby forming an at least partially oxidized layer on the substrate; and

annealing the substrate in an oxidizing ambient.

17. The method of claim 16, wherein the substrate comprises an oxidized silicon surface layer immediately prior to the depositing step.

18. The method of claim 16, wherein the substrate comprises a clean Si surface immediately prior to the depositing step.

19. The method of claim 16, wherein the depositing a first metal and silicon step comprises simultaneous deposition of a layer comprising both the first metal and silicon.

20. The method of claim 19, wherein the simultaneous deposition comprises sputtering material from a target comprised of the first metal and silicon onto the substrate.

21. The method of claim 19, wherein the simultaneous deposition comprises evaporating the first metal and silicon from a common source.

22. The method of claim 19, wherein the simultaneous deposition comprises evaporating the first metal and silicon from separate sources.

23. The method of claim 22, wherein the evaporation rate of the separate sources are independently varied during the depositing step, thereby forming a metal silicate dielectric layer having a depth-varying ratio of the first metal to silicon.

24. The method of claim 1, wherein the forming a metal silicate dielectric layer step comprises the repeated steps of:

evaporating an intermediate layer of material onto the substrate, the material selected from the group consisting of silicon, a first metal, and combinations thereof, the intermediate layer having a thickness less than 1 nanometer; and

annealing the substrate in an oxidizing ambient, thereby at least partially oxidizing the intermediate layer.

25. The method of claim 24, wherein a first set of one or more of the intermediate layers are silicon, and a second set of one or more of the intermediate layers comprise the first metal, the first set of layers and set second set of layers being deposited in alternating fashion.

26. The method of claim 1, wherein the forming a metal silicate dielectric layer step comprises:

exposing a clean Si surface on the substrate; and

depositing a partially reduced metal silicate layer on the Si surface.

27. The method of claim 26, further comprising annealing the partially reduced metal silicate layer substrate in oxygen, thereby forming the metal silicate dielectric layer.

28. The method of claim 27, wherein the depositing a partially reduced metal silicate layer on the Si surface comprises simultaneous physical vapor deposition of a metal oxide and silicon.

29. The method of claim 27, wherein the depositing a partially reduced metal silicate layer on the Si surface comprises simultaneous physical vapor deposition of zirconium oxide and silicon.

30. The method of claim 27, wherein the depositing a partially reduced metal silicate layer on the Si surface comprises simultaneous physical vapor deposition of hafnium oxide and silicon.

31. An integrated circuit having a field effect device fabricated thereon, the field effect device comprising:

a single-crystal silicon semiconducting channel region;

a metal silicate gate dielectric overlying the channel region; and

a conductive gate overlying the gate dielectric.

32. The integrated circuit of claim 31, wherein the gate dielectric is polycrystalline.

33. The integrated circuit of claim 31, wherein the gate dielectric is amorphous.

34. The integrated circuit of claim 31, wherein the metal silicate is selected from the group consisting of zirconium silicate, barium silicate, cerium silicate, zinc silicate, thorium silicate, bismuth silicate, hafnium silicate, lanthanum silicate, tantalum silicate, and combinations thereof.

35. The integrated circuit of claim 31, wherein the metal silicate gate dielectric has a graded composition comprising a relatively greater ratio of silicon to metal near the semiconducting channel region, as compared to the ratio of silicon to metal near the conductive gate.

36. An integrated circuit made by the method of claim 2.

37. An integrated circuit made by the method of claim 12.

38. An integrated circuit made by the method of claim 16.

39. An integrated circuit made by the method of claim 24.

~~40. An integrated circuit made by the method of claim 28.~~

add D3

add C1

add D4